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CERTIFICATE OF MAILING

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Attorney for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/776,356	Confirmation No.: 3184
Applicant	:	Wei-Chieh Hsueh	
Title	:	PIXEL DRIVING CIRCUIT AND METHOD FOR USE IN ACTIVE MATRIX ELECTRON LUMINESCENT DISPLAY	
Filed	:	February 11, 2004	
TC/A.U.	:	2629	
Examiner	:	Richard A. Hjerpe	
Docket No.	:	3304.2.119	
Customer No.	:	21552	



Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Transmitted herewith is an Information Disclosure Statement disclosing information which has come to the attention of applicant and/or his attorneys and is being submitted so as to comply with the duty of disclosure set forth in 37 C.F.R. § 1.56. In accordance with 37 C.F.R. § 1.97(b), the enclosed Statement is being filed within three (3) months of the filing date of the above-identified application or before the mailing date of a first Action on the merits.

Neither applicant nor his attorneys make any representation that any information disclosed herein may be "prior art" within the meaning of that term under 35 U.S.C. § 102 or § 103. Moreover, pursuant to 37 C.F.R. § 1.97, the filing of this Information Disclosure Statement

shall not be construed as a representation that a search has been made or as an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

In accordance with 37 C.F.R. § 1.98, transmitted herewith are:

1. A completed copy of Form PTO/SB/08a "Information Disclosure Statement by Applicant" listing the patents, publications and other information being submitted for consideration; and
2. A legible copy of each patent, publication and other item of information in written form listed on the enclosed Form PTO/SB/08a, except for copies of U.S. patents and published U.S. patent applications which are not required for applications filed after June 30, 2003.

NON-ENGLISH INFORMATION

Pursuant to 37 C.F.R. § 1.98, following is a concise explanation of the relevance (as it is presently understood by the individual designated in 37 C.F.R. § 1.56(c) most knowledgeable about the content of the information), of each listed patent, publication or other information that is not in the English language:

1. Japanese Patent Application No. 2003-140613 published May 16, 2003 discloses: **PROBLEM TO BE SOLVED:** To provide an active matrix type display realizing a high quality display by solving the problem of variation of current supplied to light emitting elements caused by variation of threshold voltage of transistors and the problem of an influence by an early effect. **SOLUTION:** A light emitting element (OLED), a voltage control current source (T1) for supplying a driving current to the light emitting element (OLED), and a current-voltage conversion element (T2) for detecting the driving current are arranged, and the voltage control current source (T1) is controlled based on a current value of the driving current detected by the current-voltage conversion element (T2). Moreover, a high-speed response can be realized by arranging a reference voltage source (Vs) for resetting the voltage between the terminals of the light emitting element (OLED).
2. Japanese Patent Application No. 2003-66905 published March 5, 2003 discloses: **PROBLEM TO BE SOLVED:** To solve such a problem that, related to a display device of current- writing type active matrix method, a write error occurs in a

transition period from writing time to emission time, to degrade picture quality.
SOLUTION: Appropriate combination of p-type and n-type drive transistor and switching transistor provides such pixel configuration as no writing error occurs. Further, using a single scan line raises the open area ratio of pixel.

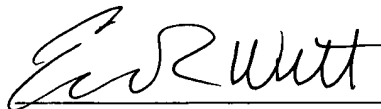
3. Japanese Patent Application No. 2003-43995 published February 14, 2003 discloses: PROBLEM TO BE SOLVED: To provide an OLED(organic light emitting diode) driving pixel circuit having satisfactory display performance. SOLUTION: In this pixel circuit, four transistors are constituted in a pixel and after first and second scanning lines GL1, GL2 which are connected respectively to the gate electrode of a second transistor MSH and that of a third transistor MWR are made active and the gate electrode and the drain electrode of a first transistor MDR are made to be in conduction state via the second transistor MSH and a current having a value corresponding to a video signal is made to flow from a power source to a signal line through the first and third transistors MDR, MWR and the first scanning line GL1 is made inactive, the second scanning line GL2 is made inactive and thereafter a third scanning line GL3 which is connected to the gate electrode of a fourth transistor MCH is made active and a current having a value corresponding to the video signal is made to flow through an OLED through the fourth transistor MCH.

CERTIFICATION UNDER 37 C.F.R. § 1.97(e)

I hereby certify that each item of information listed on the enclosed Information

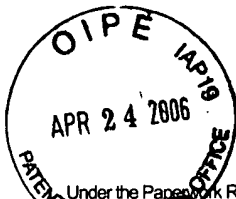
Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

Respectfully submitted,



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PTO/SB/08a (08-03)
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary) Sheet 1 Of 1		Complete if Known	
		Application Number	10/776,356
		Filing Date	February 11, 2004
		First Named Inventor	Wei-Chieh Hsueh
		Group Art Unit	2629
		Examiner Name	Richard A. Hjerpe
		Attorney Docket Number	3304.2.119

U.S. PATENT DOCUMENTS					
Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	U1	US-6,734,836	05/11/2004	Nishitoba	
	U2	US-6,859,193	02/22/2005	Yumoto	
	U3	US-6,774,877	08/10/2004	Nishitoba et al.	
	U4	US-2004/0095299	05/20/2004	Matsumoto	
	U5	US-6,693,388	02/17/2004	Oomura	
	U6	US-2003/0227262	12/11/2003	Kwon	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
	F1	JP - 2003-140613	05/16/2003	Canon KK		
	F2	JP - 2003-66905	03/05/2003	Matsushita Electric Ind. Co. Ltd.		
	F3	JP - 2003-43995	02/14/2003	Matsushita Electric Ind. Co. Ltd.		
	F4	WO - 99/65012	12/16/1999	Koninklijke Philips Electronics N.V.		

Examiner Signature		Date Considered	
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you are required to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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